IN THE ABSTRACT:

The Abstract as amended below with a replacement Abstract shows added text with underlining and deleted text with ~~strikethrough~~.

Please DELETE the Abstract in its entirety and substitute the attached new Abstract.

A branch history information write control device in an instruction execution processing apparatus includes a memory unit storing an instruction string, and a branch prediction unit performing a branch prediction of a branch instruction. A control unit in the device controls the memory unit and the branch prediction unit in such a way that writing of branch history information in the branch prediction unit and control over fetching of the instruction string in the memory unit may not occur simultaneously so that no instruction fetch is held. A bypass unit in the device makes the branch history information of the branch instruction a research target of a branch prediction, where said control unit uses a counter to count several clock cycles (several states) to delay, for a period of several clock cycles (several states), the writing of the branch history information and control, beforehand, the fetching of the instruction string.